What is claimed is:

1. A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

a photodiode region of a second conductivity type formed in the first well.

2. The sensor of claim 1, further comprising a pinning layer of the first conductivity type formed to a shallow depth in the photodiode region and electrically coupled to the substrate.

3. The sensor of claim 2, further comprising a gate electrode insulatively spaced over the first well and disposed to control a transfer of charge between the photodiode region and a predetermined region of the second conductivity type.

4. The sensor of claim 3, wherein the predetermined region of the second conductivity type is formed in the first well.

5. The sensor of claim 2, further comprising a gate electrode insulatively spaced over the substrate and disposed to control a transfer of charge between the photodiode region and a predetermined region of the second conductivity type.

6. The sensor of claim 5, further comprising a second well of the first conductivity type in the second concentration, wherein the predetermined region of the second conductivity type is formed in the second well.

7. The sensor of claim 1, further comprising a gate electrode insulatively spaced over the first well and disposed to control a transfer of charge between the photodiode region and a predetermined region of the second conductivity type.

8. The sensor of claim 7, wherein the predetermined region of the second conductivity type is formed in the first well.

9. The sensor of claim 1, wherein:

the first concentration induces the substrate to express a first intrinsic potential;

the second concentration induces the first well to express a second intrinsic potential; and

the first and second intrinsic potentials induce a field between the substrate and the first well that repels photo generated charge from drifting from the substrate into the first well.

10. The sensor of claim 1, wherein the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type in the second concentration.

11. The sensor of claim 10, wherein the CMOS process type well and the first well constitute wells formed during a single processing step, the single processing step including one of ion implantation and dopant diffusion.

12. The sensor of claim 1, wherein:

the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type; and

the CMOS process type well is formed to a greater depth than a depth of the first well.

13. The sensor of claim 1, wherein:

the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type; and

the CMOS process type well is formed to a greater concentration than the second concentration.

14. A sensor formed in a substrate of a first conductivity type comprising:

CMOS circuitry to control the sensor;

a first well of a second conductivity type formed in the substrate;

a second well of the first conductivity type formed in the first well; and

a photodiode region of the second conductivity type formed in the second well.

15. The sensor of claim 14, further comprising a pinning layer of the first conductivity type formed to a shallow depth in the photodiode region and electrically coupled to the substrate.

16. The sensor of claim 14, further comprising a gate electrode insulatively spaced over the second well and disposed to control a transfer of charge between the photodiode region and a predetermined region of the second conductivity type.

17. The sensor of claim 16, wherein the predetermined region of the second conductivity type is formed in the second well.

18. The sensor of claim 14, further comprising a bias circuit that applies a first potential to the first well and a second potential to the second well wherein the first and second potentials induce a field between the first and second wells that repels photo generated charge from drifting from the first well into the second well.

19. A method comprising steps of:

applying a first potential to a first well formed in a substrate of a first conductivity type, the substrate further having CMOS sensor control circuitry formed in the substrate, the first well being formed to have a second conductivity type; and

applying a second potential to a second well of the first conductivity type that is formed in the first well, a photodiode region of the second conductivity type being formed in the second well, wherein the first and second potentials induce a field between the first and second wells that repels photo generated charge from drifting from the first well into the second well.

20. The method of claim 19, further comprising a step of applying a third potential to a gate electrode that is insulatively spaced over the second well to enable a transfer of charge between the photodiode region and a predetermined region of the second conductivity type.

21. A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

an epi layer of the first conductivity type in a second concentration formed on the substrate, the second concentration being less than the first concentration;

a first well of the first conductivity type in a third concentration formed in the epi layer, the third concentration being greater than the second concentration; and

a photodiode region of a second conductivity type formed in the first well.

22. A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

an epi layer of the first conductivity type in a second concentration, the second concentration being less than the first concentration;

a first well of a second conductivity type formed in the epi layer;

a second well of the first conductivity type formed in the first well; and

a photodiode region of the second conductivity type formed in the second well.